



INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁷ : H02M 7/162	A1	(11) International Publication Number: WO 00/70734 (43) International Publication Date: 23 November 2000 (23.11.00)
<p>(21) International Application Number: PCT/US00/12149</p> <p>(22) International Filing Date: 4 May 2000 (04.05.00)</p> <p>(30) Priority Data: 09/310,393 12 May 1999 (12.05.99) US</p> <p>(71) Applicant: OTIS ELEVATOR COMPANY [US/US]; Intellectual Property Dept., 10 Farm Springs, Farmington, CT 06032-2568 (US).</p> <p>(72) Inventor: CZERWINSKI, Christopher, S.; 4122 Town Brooke, Middletown, CT 06457 (US).</p> <p>(74) Agents: HENLEY, Randy, G. et al.; Otis Elevator Company, Intellectual Property Dept., 10 Farm Springs, Farmington, CT 06032-2568 (US).</p>		<p>(81) Designated States: CN, JP, SG, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).</p> <p>Published <i>With international search report. Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i></p>
<p>(54) Title: CONTROL OF A DC MATRIX CONVERTER</p> <div data-bbox="449 1573 1638 1990"><p>The diagram shows three horizontal timelines labeled 'at', 'bt', and 'ct' on the left. Each timeline contains a series of vertical pulses. The 'at' timeline has a high-frequency burst of pulses in the middle. The 'bt' timeline has a high-frequency burst of pulses in the middle. The 'ct' timeline has a high-frequency burst of pulses in the middle.</p></div> <p>(57) Abstract</p> <p>A DC matrix converter having six forward current conducting power switches and six reverse current conducting power switches has the on time duration of each power switch within a pulse width modulation period controlled by relationships between d and q components of a modulation index determined by the ratio of a voltage command to the instantaneous voltage of the AC mains expressed in stationary dq coordinates, the selection of which is made based on inequalities between the DC main voltage components expressed in stationary dq coordinates. Switch selection is also performed in response to relationships of the AC main voltage components expressed in stationary dq coordinates. Zero vectors are selected to minimize the common mode voltage.</p>		

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Control of a DC Matrix Converter

Technical Field

This invention relates to controlling a direct, AC to DC matrix converter to supply controlled DC voltage to a load utilizing precisely controlled, pulse width modulation.

5 Background Art

In commonly owned, copending U.S. patent application Serial No. (OT-2672) filed contemporaneously herewith, a direct, 3-phase AC to DC matrix converter employs switches which are controlled in sequence to directly synthesize a desired average DC voltage waveform at the input terminals of the DC motor, while simultaneously distributing the DC output current among the AC input lines as a sinusoidal waveform in phase with the AC voltage. The difference between the direct DC matrix converter of said copending application and prior DC-PWM converters is that the prior converters create a DC power of a fixed voltage, much the same as a battery, and then utilized some portion of the voltage, as needed, synthesizing a correct DC voltage, on average, by means of pulse width modulation, whereas in said application, the desired voltage at the desired current is synthesized by pulse width modulation directly from the AC mains, while retaining the sinusoidal balance and unity power factor of the AC input currents.

20 In the system of said application, each switch is turned on and off in each modulation period. As is known, the switching losses in power switches occur only during transition between the non-conducting and conducting states; therefore, reducing the number of commutations will significantly reduce power losses in the switches.

Disclosure of Invention

Objects of the invention include providing pulse width modulation synthesis of DC voltage directly from three-phase AC mains with minimal commutation losses, with a minimum of calculations (processor steps), with modulation frequencies as high as 10KHz or more to provide minimal ripple in the DC voltage and current, with minimal distortion and a unity power factor at the AC mains.

This invention is predicated on my discovery that all switches in a DC matrix converter can be turned on and remain on for two out of three portions of the same or adjacent pulse width modulation periods, when operated in a proper sequence, including two voltage producing portions and one non-voltage producing portion of each pulse width modulation period.

According to this invention, the switch-on time of DC matrix power switches is determined by the ratio of an instantaneous voltage command signal, V^* , (indicative of the voltage to be provided by said DC matrix converter) to the instantaneous magnitude, V , of the three-phase AC mains in stationary dq coordinates, along with the phase relationship between the present instantaneous phase of said AC mains voltage in stationary dq coordinates and the leading and lagging boundaries of six phase sectors that span a cycle of said AC mains.

According to the invention further, the phase relationship are expressed in terms of dq quantities, using trigonometric angle-sum relationships and identified by inequalities existing between the voltages of the AC mains expressed in orthogonal dq coordinates and zero.

In still further accord with the invention, the pairs of switches to be used in each portion of a pulse width modulation

period are selected by relationships between the components of the AC mains voltage in orthogonal DQ coordinates. The invention may be implemented in DC matrix converters which supply unilateral current, bilateral current, and with or without regeneration.

5 Other objects, features and advantages of the present invention will become more apparent in the light of the following detailed description of exemplary embodiments thereof, as illustrated in the accompanying drawing.

Brief Description of the Drawings

10 Fig. 1 is a schematic block diagram of an elevator system employing a DC matrix converter controlled in accordance with the present invention.

15 Fig. 2 is a schematic diagram of a common emitter, DC matrix converter which may be controlled in accordance with the present invention.

Fig. 3 is a plot of AC mains voltage including designations of current vectors related to the present invention.

Fig. 4 is a space-vector diagram illustrating principles of the present invention.

20 Figs. 5 and 6 are diagrams illustrating various parameters of the invention in various sectors of a cycle.

Fig. 7 is a space-vector diagram illustrating inequalities used to control a DC matrix in accordance with the present invention.

25 Fig. 8 is a simplified logic flow diagram of an exemplary routine for determining switch-on durations in accordance with the invention.

Figs. 9-12 are diagrams illustrating sectors of a cycle in which various switches may be operated.

Fig. 13 is a logic flow diagram of a non-zero vector switch selection routine (simplified exemplary).

Fig. 14 is a space-vector diagram illustrating inequalities used to select zero vectors.

5 Fig. 15 is a simplified, logic flow diagram of an exemplary zero vector switch selection routine.

Fig. 16 is a series of waveforms on a common phase base, illustrating principles of the invention.

Best Mode for Carrying Out the Invention

10 Referring to Fig. 1, a DC matrix converter 18 provides current to a DC motor 19, which in this embodiment is shown mechanically connected to a sheave 20 which is connected by roping 21 to an elevator car 22 and a counterbalance 23. The DC matrix converter 18 selectively connects various pairs of the three-
15 phase AC mains a, b, c directly to the output terminals of the converter j, k. The voltage can be positive at terminal j and negative at terminal k, and conventional positive current flowing from terminal j to terminal k, such as, for instance, when the elevator is being driven upwardly with a heavy load, or terminal k can be positive,
20 terminal j negative and conventional positive current flowing from k to j, such as, for instance, when the elevator is being driven downwardly with a light load; this is called "motoring". Whenever the elevator is traveling upwardly with a light load, downwardly with a heavy load, or is decelerating, the sheave 20 will actually drive the
25 motor 19 so that the motor 19 acts as a generator. In such a case, the positive current flow through the motor 19 will be of opposite polarity from the polarity of voltage at the terminals j, k; this is called "regeneration". The DC matrix converter 18 will connect the switches appropriately in dependence upon magnitude and direction

of a speed command provided to the DC matrix converter controller of Fig. 1, and whether the motor 19 is operating in a motoring mode or in a regeneration mode.

5 In the example herein, the commands which will ultimately cause the DC matrix converter to drive the motor 19 in a desired fashion are provided by a conventional elevator motion controller (not shown) which provides a speed command on a line 30 to a summer 31 which subtracts the actual speed on the line 32 provided by a conventional position and speed conversion circuit 33 in
10 response to a signal on a line 34 from a suitable, conventional encoder (not shown) which is coupled to the sheave 20 (or the motor 19, as the case may be). A position output of the circuit 33 on a line 37 is fed back to the motion controller so as to determine the continuity of commands necessary to cause the elevator to move
15 in the desired fashion, all as is well known in the art and forms no part of the present invention. The output of the summer 31 is provided on a signal line 40 to a conventional speed error proportional and integral gain circuit 41, the output of which on a line 42 comprises a current command, I^* , which is fed to a summer
20 43. The summer 43 subtracts the actual motor current on a line 44, derived from a conventional current sensor 45 to provide a current error signal on a line 46. The current error signal is processed with conventional proportional and integral gain in a circuit 51, the output of which on a line 52 comprises a voltage command, V^* .

25 In accordance with the invention, the ratio of the magnitude of the voltage command to the magnitude of the input AC mains voltage vector, in stationary dq coordinates, determines a modulation index, m^* , which is used to determine the duration of switch-on time during pulse width modulation of the voltage on the AC input mains

in order to achieve the desired DC voltage for application to the load, such as the motor 19.

The voltage on the AC mains a, b, c is fed to a conventional stationary three-phase to stationary dq coordinate conversion circuit 56 to provide outputs V_d , V_q which define the three-phase input voltages of the AC mains in orthogonal coordinates, as is known. The magnitude of the AC mains, V , on a line 57, is simply the square root of the sum of the squares of V_d , V_q , performed in a conventional unit 58. The orthogonal magnitudes V_d , V_q are also fed to a conventional phase locked loop 63, the output of which on lines 65 and 66 are signals indicative of $\sin\theta$ and $\cos\theta$, respectively. These are applied to a circuit 68 which converts the modulation index m^* in synchronous dq coordinates to desired modulation index components m_q , m_d in stationary dq coordinates. The m_q and m_d signals on lines 71, 72 are fed to a duration and selection function 73 which determines the duration for which a selected pair or set of switches should be turned on, and selects which pair or set of switches are to be on, at any given moment, to perform the necessary pulse width modulation in order to synthesize the desired DC voltage at the output terminals, j, k, of the DC matrix converter 18. The functions 73 are described more fully hereinafter. Signals indicative of the duration of switch on times, and the selected pair of switches to be turned on, are provided over a trunk of lines 77 to timing circuits 78 which actually count pulses in real time so as to implement the desired durations by providing switch on gating circuits over a trunk of 12 lines 79 to the DC matrix converter 18. The timing circuits turn the switches on and off according to conventional commutation methods, so that each of the output terminals is always connected to an AC main, with no open circuit gaps, to satisfy the known continuity of current constraint. One

commutation example is set forth in Holmes and Lipo,
"Implementation of a Controlled Rectifier Using AC-AC Matrix
Converter Theory", IEEE Trans. Power Elec., Jan., 1992.

Although not shown in Fig. 1, the DC matrix converter of the
invention requires line-to-line capacitance across the AC input to
support switch commutation described hereinafter. These may be
included along with in-line inductors within an input filter 82.
Similarly, the DC matrix converter preferably has an output filter 83
with series inductance and shunt capacitance, both filters being
shown in the aforementioned application.

One embodiment of a DC matrix converter 18 is illustrated in
Fig. 2. For each phase of the AC mains, a, b, c there are two power
transistor switches at the top of Fig. 2 and two switches at the
bottom of Fig. 2. One switch at the top of Fig. 2, at+, bt+, ct+
will conduct current from the corresponding one of the AC mains
through the terminal j to the motor 19 while one of the
corresponding bottom switches ab+, bb+, cb+ will conduct current
from the motor 19, through the terminal k to the corresponding one
of the AC mains. For purposes of illustration herein, flow of current
from the terminal j, downwardly through the motor 19 to the
terminal k is deemed to be positive current flow. For negative
current flow, one of the negative bottom switches ab-, bb-, cb- will
conduct current from the corresponding one of the AC mains,
through the terminal k, through the motor 19, to the terminal j, and
one of the top negative switches at-, bt-, ct- will conduct current
from the terminal j to a corresponding one of the AC mains.

The general nature of operation of the DC matrix converter is
illustrated in Fig. 3. Therein, the sinusoidal voltage of the AC mains
 V_a , V_b , V_c is plotted against time. Also plotted in Fig. 3 are a
plurality of different current vectors i_1 , i_2 ... i_6 which can result from

various combinations of conducting power transistor switches at + ,
 bt + ...cb- in Fig. 2. These appear as vertical arrows extending from
 a negative voltage to a positive voltage. Associated with each
 vertical arrow is a horizontal arrow bearing the same designation in
 parenthesis, which indicates the portion of each cycle within which
 5 the corresponding current vector may be switched (about fifty-five
 times per cycle in the example hereinafter) to produce positive
 voltage at the output terminals ($V_j > V_k$) whenever the input
 command is positive ($m^* > 0$). In each instance, the top portion of
 10 the arrow is designated as current flowing through a switch
 designated a, b or c, the designation At indicating that either the
 transistor at + or the transistor at- will be conducting at that
 particular time, depending upon whether current flow is to be
 positive or negative, as described hereinbefore. Similarly, the
 15 designation Cb for the current vector i1 indicates that one of the
 transistors cb + , cb- , will be conducting in dependence upon
 whether the current flow is to be positive or negative, respectively.
 Thus, for the current vector i1 (whether it be positive or negative, as
 described hereinafter) is achieved by connecting phase c of the AC
 -20 mains and phase a of the AC mains to the terminals k and j of the
 matrix, respectively. The current vector i1 can exist in time from the
 point where $V_c = 0$ to the point where $V_a = 0$.

The commanded modulation index, m^* for the DC matrix
 converter is transformed to the stationary reference frame, in dq
 25 coordinates, as follows:

$$\begin{aligned} m_d &= m^* \sin \theta \\ m_q &= m^* \cos \theta \quad 0 < \theta < 2\pi \end{aligned}$$

where $\Theta = 0$ corresponds to the q-axis of the AC mains voltage in the synchronous reference frame (63-68, Fig. 1).

The currents i_1 - i_6 are the only possibilities that produce non-zero voltage at the output terminals (V_j not equal to V_k), which can be achieved by selective operation of two of the switches in Fig. 2 at one time. For instance, if switch a_t+ is operated simultaneously with switch b_b+ in Fig. 2, this will result in current i_6 as illustrated in Fig. 3. If a_t+ is operated simultaneously with c_b+ , this will result in current i_1 of Fig. 3. If a_t+ is operated simultaneously with a_b+ , this short circuits the terminals j, k with no differential voltage produced at the output terminals ($V_j = V_k$), with current circulating through the a_t+ and a_b+ switches, which is defined herein as a zero vector. The synthesis of the DC voltage is accomplished by pulse width modulation at a frequency which is very high with respect to the frequency of the AC mains, such as 10KHz, resulting in a short modulation period, such as $100\mu s$. Within each $100\mu s$ modulation period, a first pair of switches (such as A_t, B_b) will be conducting for some fraction of the modulation period (defined as "duty ratio" and as "duration"), a second pair of switches (such as A_t, C_b) will be conducting for some portion of that modulation period, and a zero vector formed by a set of switches related to the same phase, such as B_t, B_b will be conducting for the remaining fraction of time to provide a zero vector, as described hereinafter.

Referring to Fig. 4, a space vector diagram, illustrating the methodology for controlling the DC matrix converter, includes each of the current vectors i_1 - i_6 which result from turning on a selected pair of switches, as described hereinbefore. The current vectors i_1 - i_6 are boundaries separating six phase sectors, $s = 0, \dots s = 5$. Each boundary is a lagging boundary for one phase sector and a

leading boundary for the next following phase sector. In Fig. 4, a particular torque current reference, i^* , for a case when positive output voltage is to be produced ($m^* > 0$), is illustrated within a modulation period which exists at a point in time when i_6 may be utilized and when i_1 may be utilized. This is defined as phase sector zero ($s = 0$). The resulting modulation index m^* and related quantities m_d , m_q are also shown. For the modulation period depicted in Fig. 4, a leading current vector (or boundary) defined as i_α is the current vector i_6 , and a lagging current vector (or boundary) defined as i_β is the current vector i_1 . The duty ratios, or durations of time, d_α , d_β , that pairs of switches are turned on, for corresponding current vectors i_α , i_β , in order to approximate the reference vector, i^* , is proportional to the sine of the angle between the reference vector and the corresponding leading and lagging current vectors i_α , i_β . The duty ratios to be used in each sector are given by

$$d_\alpha = m^* \sin(\pi/3 - \phi) \quad d_\beta = m^* \sin(\phi) \quad 0 < \phi < \pi/3$$

$$d_0 = 1 - d_\alpha - d_\beta,$$

where $\phi = 0$ and $\phi = \pi/3$ correspond to the angular location of the α -vector and β -vector, respectively.

In further accord with the invention, to determine the switch times, the above modulation functions are expressed in terms of dq quantities by using trigonometric angle-sum relations in each sector as follows. Using the above equations and the fact that

$\phi = \pi/6 + \Theta - s\pi/3$, where s is the sector in Fig. 4, for $0 < s < 5$, one can express

5
$$\begin{aligned} d\alpha &= m' \sin\{\pi/3 - (\pi/6 + \Theta - s\pi/3)\} = m' \sin(\pi/6 + s\pi/3 - \Theta) \\ &= m' \sin(\pi/6 + s\pi/3) \cos\Theta - m' \cos(\pi/6 + s\pi/3) \sin\Theta \\ &= \sin(\pi/6 + s\pi/3) m_q - \cos(\pi/6 + s\pi/3) m_d \end{aligned}$$

and

$$\begin{aligned} d\beta &= m' \sin\{\pi/6 + \Theta - s\pi/3\} = m' \sin(\pi/6 - s\pi/3 + \Theta) \\ &= m' \sin(\pi/6 - s\pi/3) \cos\Theta + m' \cos(\pi/6 - s\pi/3) \sin\Theta \\ &= \sin(\pi/6 - s\pi/3) m_q + \cos(\pi/6 - s\pi/3) m_d \end{aligned}$$

10 For reference, the values of the sine and cosine coefficients in the above equations are given in the following table, for each sector $s=0$ through $s=5$.

15

s	$\sin(\pi/6 + s \pi/3)$	$-\cos(\pi/6 + s \pi/3)$	$\sin(\pi/6 - s \pi/3)$	$\cos(\pi/6 - s \pi/3)$
0	$\frac{1}{2}$	$-\sqrt{3}/2$	$\frac{1}{2}$	$\sqrt{3}/2$
1	1	0	$-\frac{1}{2}$	$\sqrt{3}/2$
2	$\frac{1}{2}$	$\sqrt{3}/2$	-1	0
3	$-\frac{1}{2}$	$\sqrt{3}/2$	$-\frac{1}{2}$	$-\sqrt{3}/2$
4	-1	0	$\frac{1}{2}$	$-\sqrt{3}/2$
5	$-\frac{1}{2}$	$-\sqrt{3}/2$	1	0

If the following quantities are defined:

$$m1 = \frac{\sqrt{3}}{2} m_d - \frac{1}{2} m_q$$

5

$$m2 = \frac{\sqrt{3}}{2} m_d + \frac{1}{2} m_q$$

then the modulation functions (α and β duty ratios) are determined in each sector by the quantities given in the following table:

10

s	$d\alpha$	$d\beta$
0	-m1	m2
1	m _q	m1
2	m2	-m _q
3	m1	-m2
4	-m _q	-m1
5	-m2	m _q

15

This is illustrated in the space-vector diagrams of Figs. 5 and 6. Thus, the duty cycles for both vectors $d\alpha$ and $d\beta$ are determined solely by the quantities m_q , $m1$ and $m2$, which can be easily calculated on a digital signal processor using the foregoing equations as shown in steps 101-104 in Fig. 8.

20

During a modulation period which is at the beginning of a sector, the switching time for the α vector will be significant, and the switching time for the β vector will be slight. Midway through the sector, the switching time for the α vector will be equal to the switching time of the β vector. Near the end of a sector, the on-time

25

for the β vector will be significant and the on-time for the α vector will be slight. In the remainder of each modulation period, $d0 = 1-d\alpha-d\beta$ (the duration for the zero vector), a pair of switches related to the same AC main, such as Bt, Bb, will be turned on so as to provide a zero vector, thereby adjusting the magnitude of the output voltage while utilizing a minimum number of switch commutations. The times when the various top switches will be turned on so as to conduct an α vector are shown in Fig. 9, and the times to conduct a β vector are shown in Fig. 10. The times the various bottom switches are turned on so as to conduct an α vector are shown in Fig. 11, and the times when they are turned on so as to conduct a β vector are shown in Fig. 12. When to apply each quantity (m_q , m_1 , m_2) necessitates a determination of the sector in which the AC mains input voltage vector lies, which is accomplished with inequality testing, and testing whether m^* is positive or negative. The inequalities that define the sector boundaries for $m^* > 0$ are shown in Fig. 7. Therein, V_d and V_q refer to the input AC mains voltage in stationary coordinates (56, Fig. 1). For negative commands ($m^* < 0$) the current vector I^* is shifted by π radians from that shown in Fig. 4. The following table shows the quantities to use in selecting the top and bottom α and β switches.

	$m^* > 0$	$m^* < 0$
Top Switches	$V_d' = V_d$ $V_q' = V_q$	$V_d' = -V_d$ $V_q' = -V_q$
Bottom Switches	$V_d' = -V_d$ $V_q' = -V_q$	$V_d' = V_d$ $V_q' = V_q$

Therefore, test 107 and steps 108-111 define V_d' and V_q' appropriately for the sign of m^* before the inequalities are tested.

- 14 -

From Fig. 6, $|d\beta| = m_2$ in sectors 0 and 3, which are defined by the following inequality:

$$\begin{aligned} & [V_d > -V_q/\sqrt{3} \cap V_d < V_q/\sqrt{3}] \cup [V_d < -V_q/\sqrt{3} \cap V_d > V_q/\sqrt{3}] \\ & [|V_d| < V_q/\sqrt{3}] \cup [|V_d| < -V_q/\sqrt{3}] \\ 5 \quad & |V_d/\sqrt{3}| < |V_q| \end{aligned}$$

This is easily tested for on a digital signal processor as shown in test 115 of Fig. 8. Similarly, $|d\beta| = m_1$ in sectors 1 and 4, which are defined by the following inequality:

$$\begin{aligned} & [V_q < 0 \cap V_d < V_q/\sqrt{3}] \cup [V_q > 0 \cap V_d > V_q/\sqrt{3}] \\ 10 \quad & [V_d V_q > V_q^2/\sqrt{3}] \cup [V_d V_q > V_q^2/\sqrt{3}] \\ & V_d V_q/\sqrt{3} > V_q^2 \end{aligned}$$

This is determined in test 116 of Fig. 8.

The remaining sectors, 2 and 5, in which $|d\beta| = m_q$, are determined through the process of elimination (tests 115 and 116 negative, Fig. 8). The sign of $d\beta$ is determined by testing the sign of V_q in tests 117-119 of Fig. 8; i.e., $d\beta = -d\beta$ if $V_q < 0$, as shown in steps 120-122, Fig. 8.

The duty ratio $d\alpha$ is easily obtained by noting in Fig. 5 that $d\alpha$ is shifted $2\pi/3$ radians relative to $d\beta$ in Fig. 6. Hence, the determination of $d\alpha$ is identical to the assignments above by using the following substitution when testing the above inequalities:

- 15 -

$$v_d'' = -\frac{1}{2} v_d' - \frac{\sqrt{3}}{2} v_q'$$

5

$$v_q'' = -\frac{1}{2} v_q' + \frac{\sqrt{3}}{2} v_d'$$

10 This is achieved by steps 123 and 124 (Fig. 8) which make the substitution, and steps and tests 125 which repeat steps and tests 115-122, etc.

Once the on-times are determined for the α and β vectors, it is necessary to determine which switches are to be turned-on to produce the vectors according to Fig. 4. This is a two-step process:
15 a determination of switches for the non-zero vectors, followed by switch assignments for the zero vector.

The phases (i.e., switches) to which the above duty ratios or durations apply are determined by the region in which the voltage vector lies. For example, the switch assignments for the top power switches in the DC matrix converter for the α vector and β vector are shown in Figs. 9 and 10. If the vector lies in one of the sectors denoted Bt, then the switch assignment is made to Bt. Referring to Fig. 10, for switch Bt, the sectors $s = 1$ or $s = 2$ can be jointly identified by testing the following inequality (test 130, Fig. 13):

25
$$[v_d' > -v_q' \sqrt{3}] \cap [v_d' > v_q' \sqrt{3}]$$

$$v_d' \sqrt{3} > |v_q'|$$

The remaining assignments of top switches for the β -vector are determined, after eliminating sectors 1 and 2, by testing the sign of V_q as shown in Fig. 7; if $V_q' > 0$ (test 131 affirmative), the sector is 0 or 5 and the top β switch is At; if $V_q < 0$ (test 131 negative),
30 the sector is 3 or 4, and the top β switch is Ct.

The top switch assignments for the α -vector are easily obtained by noting in Fig. 9 the phase shift of $\pi/3$ radians relative to the top switch assignment for the β -vector in Fig. 10. Hence, the determination of the top switch for the α -vector is identical to the assignments above if the following substitutions are first made

5 (steps 135, 136, Fig. 13):

$$V_{d'} = 1/2 V_{d'} - \sqrt{3}V_{q'}/2$$

$$V_{q'} = -1/2 V_{q'} + \sqrt{3}V_{d'}/2$$

These assignments are shown in tests and steps 138 of Fig. 13.

10 Determination of bottom switch assignments for the α -vector and β -vector is identical to the above except for a phase shift of π radians between the assignments for the two groups. Hence, the determination is identical to the above when using the following substitutions (steps 140, 141, Fig. 13):

15 $V_{d''} = -V_{d''}$

$$V_{q''} = -V_{q''}$$

These selections are made in steps and tests 143 of Fig. 13.

As described hereinbefore, a zero vector, i_0 , is defined as the short circuiting of the output terminals j, k by a set of like-phase

20 switches, At, Ab; Bt, Bb; Ct, Cb. The selection of which set of switches to use in representing the zero vector affects the common-mode output voltage. The application of each vector, $i_1 - i_6$, results in each of the output terminals, j, k, to be connected to one of the AC main voltages V_a , V_b , or V_c . The differential voltage applied

25 across the load, V_D , is the difference in the output phase voltages, $V_j - V_k$, while the common-mode voltage referenced to the system neutral, V_{CM} , is the sum of the two output line voltages divided by

the number of output phases, $(V_j + V_k)/2$. The resulting differential and common-mode voltages produced by each vector is given in the following tables:

5

Vector	i1	i2	i3	i4	i5	i6
Switches	At,Cb	Bt,Cb	Bt,Ab	Ct,Ab	Ct,Bb	At,Bb
Vj	VC	VC	VA	VA	VB	VB
Vk	VA	VB	VB	VC	VC	VA
VD	VAC	VBC	VBA	VCA	VCB	VAB
VCM	$\frac{VA+VC}{2}$	$\frac{VB+VC}{2}$	$\frac{VB+VA}{2}$	$\frac{VC+VA}{2}$	$\frac{VC+VB}{2}$	$\frac{VA+VB}{2}$

10

Vector	i0	i0	i0
Switches	At,Ab	Bt,Bb	Ct,Cb
Vj	VA	VB	VC
Vk	VA	VB	VC
VD	0	0	0
VCM	VA	VB	VC

15

Since the line voltages V_a , V_b , and V_c are sinusoidal, the peak common-mode voltage attained by the non-zero vectors, i_1 through i_6 , over an AC cycle is easily calculated as

20

$$V_{CM} \text{ (peak)} = 1/2\sqrt{2/3} V_{LL}, 0 < \omega t \leq 2\pi$$

where V_{LL} is the rms line-to-line voltage and ωt is the AC phase angle in radians. In contrast, the peak common-mode voltage attained by the zero vectors during the same period is

25

$$V_{CM} \text{ (peak)} = \sqrt{2/3} V_{LL}, 0 < \omega t \leq 2\pi$$

As a consequence, an indiscriminant use of the zero vectors results in a peak common-mode voltage which is twice that for the non-zero vectors.

5 The zero vectors can, however, be chosen in such a way as to reduce the peak common-mode voltage. For example, if the use of the zero vector (A_t , A_b) is restricted to the periods

$$\frac{\pi}{3} \leq \omega t \leq \frac{2\pi}{3} \quad \text{and} \quad \frac{4\pi}{3} \leq \omega t \leq \frac{5\pi}{3}$$

where $\omega t = 0$ corresponds to the peak of the line voltage V_a , the maximum common mode voltage is given by:

10
$$V_{CM}(peak) = \sqrt{\frac{2}{3}} V_{LL} \cos\left(\frac{\pi}{3}\right), \quad \frac{\pi}{3} < \omega t \leq \frac{2\pi}{3} \text{ or } \frac{4\pi}{3} < \omega t \leq \frac{5\pi}{3}$$

which equals

$$V_{CM}(peak) = \frac{1}{2} \sqrt{\frac{2}{3}} V_{LL}, \quad \frac{\pi}{3} < \omega t \leq \frac{2\pi}{3} \text{ or } \frac{4\pi}{3} < \omega t \leq \frac{5\pi}{3}$$

15 Consequently, the peak common-mode voltage produced by this zero vector has been reduced by half, by restricting its usage during the AC cycle. To realize this reduction factor over the entire AC cycle, similar restrictions are placed on the other zero vectors. This is summarized in the following table and illustrated in Fig. 14.

Zero Vector	Allowable Periods of Application
(At, Ab)	$\pi/3 < \omega t < 2\pi/3$ and $4\pi/3 < \omega t < 5\pi/3$
(Bt, Bb)	$0 < \omega t < \pi/3$ and $\pi < \omega t < 4\pi/3$
(Ct, Cb)	$2\pi/3 < \omega t < \pi$ and $5\pi/3 < \omega t < 0$

- 5 Determination of the switch sets for the zero vector, denoted SW0, applies to both the top and bottom groups of switches in the DC matrix converter. Determination of which sector the voltage vector lies in is accomplished with inequality testing. The inequalities that define the sector boundaries are shown in Fig. 14.
- 10 The sectors, in which SW0 = A, are defined by the following inequality (positive result of test 139 of Fig. 15):

$$\begin{aligned}
 & [v_d > -v_q\sqrt{3} \cap v_d > v_q\sqrt{3}] \cup [v_d < -v_q\sqrt{3} \cap v_d < v_q\sqrt{3}] \\
 & [v_d > |v_q\sqrt{3}|] \cup [-v_d > |v_q\sqrt{3}|] \\
 & |v_d| > |v_q\sqrt{3}|
 \end{aligned}$$

- 15 Similarly, SW0 = B is identified by testing the following inequality (positive result of test 140 of Fig. 15);

$$\begin{aligned}
 & [v_d > 0 \cap v_d < v_q\sqrt{3}] \cup [v_d < 0 \cap v_d > v_q\sqrt{3}] \\
 & [v_d^2 < v_d v_q\sqrt{3}] \cup [v_d^2 < v_d v_q\sqrt{3}] \\
 & v_d^2 < v_d v_q\sqrt{3}
 \end{aligned}$$

- 20 SW0 = C is determined by elimination (negative result of test 140 of Fig. 15).

If desired, programming may be simplified by noting the similarity to the algorithm for setting the duty ratios, provided the following substitution is made:

$$V_d = V_q$$

5

$$V_q = V_d$$

The zero vector switch selection described hereinbefore with respect to Figs. 14 and 15 is disclosed and claimed in commonly owned copending U.S. patent application Serial No. (OT-4208), filed contemporaneously herewith.

10

Within each modulation period, the order in which the various pairs and sets of switches are operated for the α vector, the β vector, and the zero vector, is immaterial. Thus the order may be α , β , zero; β , α , zero; β , zero, α ; or any other order. With the constraint that a switch conducting between one of the AC mains and one of the output terminals is never shut off until another switch is turned on to conduct from an AC main to that terminal, the relationship of switch pairs (α and β) and sets (zero vectors) illustrated in Fig. 4 (along with Figs. 9-12 and 14) show that switch commutation is minimized by practicing the present invention. For instance, switch At will be turned on as part of the α vector when the α vector is i_6 (comprising the leading boundary of phase sector $s = 0$), and remain on during the β portion of each modulation period as part of the pair for current vector i_1 . On the other hand, switch At may be first turned on as part of current vector i_1 and remain on as part of current vector i_6 , within each of the modulation periods within the phase sector, $s = 0$. And even if the zero vectors switch set is operated between the pair of α switches and the pair of β switches, in one modulation period, the At switch, for instance, may be turned on for i_6 at the end of one modulation period, and remain on for i_1 in the beginning of the next following modulation period. Thus, in any

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case, two switches will be turned on only once per modulation period, in contrast with three switches being turned on per modulation period in any schemes heretofore known to the prior art. Thus, the number of commutations for switches in forming the non-zero vectors is reduced by one-third. The same relationships exist for the zero vector commutations.

Thus, the advantages of reduced commutations offered by the space-vector approach of the invention represented in the space-vector diagram shown in Fig. 4 may be combined with the reduced requirements of common-mode magnetic components offered by reduced common-mode voltage realized by curtailing the allowable periods of application for the zero vectors, shown in said copending application Serial No. (OT-4208). The combined strategy of all allowable vectors, for $m^* > 0$, is given in the following table.

Sector	Vector I_α	Vector I_β	Angle	Voltage Relationship	Zero Vector
0	i6 (A1,B2)	i1 (A1,C2)	330-360	$V_A > V_C > V_B$	(C1,C2)
			0-30	$V_A > V_B > V_C$	(B1,B2)
1	i1 (A1,C2)	i2 (B1,C2)	30-60	$V_B > V_A > V_C$	(A1,A2)
			60-90		
2	i2 (B1,C2)	i3 (B1,A2)	90-120	$V_B > V_C > V_A$	(C1,C2)
			120-150		
3	i3 (B1,A2)	i4 (C1,A2)	150-180	$V_C > V_B > V_A$	(B1,B2)
			180-210		
4	i4 (C1,A2)	i5 (C1,B2)	210-240	$V_C > V_A > V_B$	(A1,A2)
			240-270		
5	i5 (C1,B2)	i6 (A1,B2)	270-300	$V_A > V_C > V_B$	(C1,C2)
			300-330		

Referring to Fig. 4, at small phase angles ϕ within sector 0, within each pulse width modulation period, switch A_t is on for a relatively long time (along with a switch B_b) in relation to the α vector I₆, and it is on for a relatively short time (along with a switch

Cb) in relation to the β vector, I1. At large phase angles ϕ within sector zero, the opposite occurs. The switch At remains continuously on for the portions related both to the α vector and the β vector. In the center of sector 0, the time that the At switch remains on is maximal, giving rise to the duty cycle waveform of Fig. 16(a). Fig. 16(b) shows an exemplary set of on times for switches at, bt and ct, and Fig. 16(c) illustrates the instantaneous (unfiltered, idealized) DC output voltage that would result.

The order in which the calculations are performed (Figs. 8, 13 and 15) is irrelevant to the present invention. Of course, the switch selection (each pair or set) as well as the duration for each pair or set has to be known before that pair or set can be operated in each modulation period. The use of the selection and duration information within the timing circuit 78 is conventional, being essentially the same as is utilized in AC-AC matrix converters.

The invention has been described in an embodiment in which there are 12 switches at+ at-, ... cb+, cb-, in order to accommodate loads in both directions and regeneration. However, the invention may as well be utilized in DC matrix converters driving loads in a single direction without regeneration, such as for driving power tools, or in other applications.

The present invention has been shown as it may be implemented utilizing n-type, punch-through, insulated gate bipolar transistor power switches. However, the invention may be implemented using p-type transistors, or with non-punch-through, insulated gate bipolar transistors connected in anti-parallel pairs.

The foregoing patent application and article are incorporated herein by reference.

I claim:

- 23 -

Claims

1. A method of controlling the flow of current through a DC matrix converter between a DC load and a set of three-phase AC mains, said DC matrix converter comprising a plurality of top switches, each connected between a corresponding one of said AC mains and a first DC output of said DC matrix converter, and a
5 plurality of bottom switches, each connected between a corresponding one of said AC mains and a second DC output of said DC matrix converter, comprising:

operating said switches in a manner so that each switch,
10 when operated to connect a corresponding one of said AC mains to a related specific one of said DC outputs, remains operated until another switch has operated to connect one of said AC mains to said specific DC output, and so that one of said top switches is operated contemporaneously with one of said bottom switches, said switches
15 being operated in pairs, each pair including a top switch related to one AC main and a bottom switch related to an AC main other than said one AC main, and said switches also being operated in sets, each set including a top switch and a bottom switch both related to the same AC main;

20 providing a voltage command signal, V^* , indicative of the voltage to be provided by said DC output terminals to said load;

providing a modulation command, m^* , as the ratio of said voltage command signal, V^* , to the instantaneous magnitude of voltage, V , of said AC mains in stationary d, q coordinates; and

25 providing an in-phase modulation command component, $m_q = m^* \cos\theta$ and a quadrature modulation command component $m_d = m^* \sin\theta$;

providing a quantity $m_1 = \sqrt{3}m_d/2 - m_q/2$;

providing a quantity $m_2 = \sqrt{3}m_d/2 + m_q/2$;

30 providing an in-phase component, V_q , and a quadrature component, V_d , of the instantaneous AC mains voltage in orthogonal coordinates aligned with the phase of a given one of said AC mains; and

providing, when $|V_d\sqrt{3}| < |V_q|$, a first fraction
 35 $d\alpha = -m_1$ if $V_q > 0$ and $d\alpha = m_1$ if $V_q < 0$, and a second fraction $d\beta = m_2$ if $V_q > 0$ and $d\beta = -m_2$ if $V_q < 0$;

providing when $V_d V_q \sqrt{3} > V_q^2$, said first fraction $d\alpha = -m_2$ if $V_q > 0$ and $d\alpha = m_2$ if $V_q < 0$, and said second fraction $d\beta = m_q$ if $V_q > 0$ and $d\beta = -m_q$ if $V_q < 0$; and

40 providing, when neither $|V_d\sqrt{3}| < |V_q|$ nor $V_d V_q \sqrt{3} > V_q^2$, said first fraction $d\alpha = m_q$ if $V_q > 0$ and $d\alpha = -m_q$ if $V_q < 0$, and said second fraction $d\beta = -m_1$ if $V_q > 0$ and $d\beta = -m_1$ if $V_q < 0$; and

in each of a continuous sequence of modulation periods
 45 which are small compared with the period of voltage of said AC mains, operating a first pair of said switches for said first fraction, $d\alpha$, of said period, operating a second pair of said switches for said second fraction, $d\beta$, of said period, and operating a set of switches for the remainder of said period.

2. A method according to claim 1 wherein said first fraction of time precedes said second fraction of time within said modulation periods.

3. A method according to claim 1 wherein the remainder of said period follows said first and second fractions of time within said modulation periods.

- 25 -

4. A method of controlling the flow of current through a DC matrix converter between a DC load and a set of three-phase AC mains, said DC matrix converter comprising a plurality of top switches, each connected between a corresponding one of said AC mains and a first DC output of said DC matrix converter, and a plurality of bottom switches, each connected between a corresponding one of said AC mains and a second DC output of said DC matrix converter, comprising:

operating said switches in a manner so that each switch, when operated to connect a corresponding one of said AC mains to a related specific one of said DC outputs, remains operated until another switch has operated to connect one of said AC mains to said specific DC output, and so that one of said top switches is operated contemporaneously with one of said bottom switches, said switches being operated in pairs, each pair including a top switch related to one AC main and a bottom switch related to an AC main other than said one AC main, and said switches also being operated in sets, each set including a top switch and a bottom switch both related to the same AC main;

in each of a continuous sequence of modulation periods which are small compared with the period of voltage of said AC mains, operating a first pair of said switches for a first fraction, $d\alpha$, of said period, operating a second pair of said switches for a second fraction, $d\beta$, of said period, and operating a set of switches for the remainder of said period;

characterized by the improvement comprising:

providing an in-phase component, V_q , and a quadrature component, V_d , of the instantaneous AC mains voltage in orthogonal coordinates aligned with the phase of a given one of said AC mains;

30 if $V_d\sqrt{3} < |V_q|$, said first pair of switches include a top
switch connected to a third AC main, next advanced in phase from
said given one of said AC mains, but if not, then if $V_q > 0$, said first
pair of switches include a top switch connected to said given one of
said AC mains, but if neither, then said first pair of switches include
35 a top switch connected to a second AC main, next delayed in phase
from said given one of said AC mains;

 if $V_d\sqrt{3} > |V_q|$, said first pair of switches include a
bottom switch connected to said third AC main, but if not, then if -
 $V_q < 0$, said first pair of switches include a bottom switch
40 connected to said given one of said AC mains, but if neither, then
said first pair of switches include a bottom switch connected to said
second AC main;

 if $V_d\sqrt{3} > |V_q|$, said second pair of switches include a top
switch connected to said second main, but if not, then if $V_q > 0$,
45 said second pair of switches include a top switch connected to said
given one of said AC mains, but if neither, then said second pair of
switches include a top switch connected to said third AC main; and

 if $V_d\sqrt{3} < |V_q|$, said second pair of switches include a
bottom switch connected to said second main, but if not, then if V_q
50 < 0 , said second pair of switches include a bottom switch
connected to said given one of said AC mains, but if neither, then
said second pair of switches include a bottom switch connected to
said third AC main.

5. A method according to claim 4 wherein said first fraction
of time precedes said second fraction of time within said modulation
periods.

6. A method according to claim 4 wherein the remainder of said period follows said first and second fractions of time within said modulation periods.

7. A method of controlling the flow of current through a DC matrix converter between a DC load and a set of three-phase AC mains, said DC matrix converter comprising a plurality of top switches, each connected between a corresponding one of said AC mains and a first DC output of said DC matrix converter, and a plurality of bottom switches, each connected between a corresponding one of said AC mains and a second DC output of said DC matrix converter, comprising:

operating said switches in a manner so that each switch, when operated to connect a corresponding one of said AC mains to a related specific one of said DC outputs, remains operated until another switch has operated to connect one of said AC mains to said specific DC output, and so that one of said top switches is operated contemporaneously with one of said bottom switches, said switches being operated in pairs, each pair including a top switch related to one AC main and a bottom switch related to an AC main other than said one AC main, and said switches also being operated in sets, each set including a top switch and a bottom switch both related to the same AC main;

providing a voltage command signal, V^* , indicative of the voltage to be provided by said DC output terminals to said load;

providing a modulation command, m^* , as the ratio of said voltage command signal, V^* , to the instantaneous magnitude of voltage, V , of said AC mains in stationary d, q coordinates; and

providing an in-phase modulation command component,

- 28 -

$m_q = m^* \cos \theta$ and a quadrature modulation command component
 $m_d = m^* \sin \theta$;

providing a quantity $m_1 = \sqrt{3}m_d/2 - m_q/2$;

providing a quantity $m_2 = \sqrt{3}m_d/2 + m_q/2$;

30 providing an in-phase component, V_q , and a quadrature component, V_d , of the instantaneous AC mains voltage in orthogonal coordinates aligned with the phase of a given one of said AC mains; and

providing, when $|V_d\sqrt{3}| < |V_q|$, said first fraction

35 $d\alpha = -m_1$ if $V_q > 0$ and $d\alpha = m_1$ if $V_q < 0$, and said second fraction $d\beta = m_2$ if $V_q > 0$ and $d\beta = -m_2$ if $V_q < 0$;

providing when $V_d\sqrt{3} = V_q$, said first fraction $d\alpha = -m_2$ if $V_q > 0$ and $d\alpha = m_2$ if $V_q < 0$, and said second fraction $d\beta = m_q$ if $V_q > 0$ and $d\beta = -m_q$ if $V_q < 0$; and

40 providing, when neither $|V_d\sqrt{3}| < |V_q|$ nor $V_d\sqrt{3} = V_q$, said first fraction $d\alpha = m_q$ if $V_q > 0$ and $d\alpha = -m_q$ if $V_q < 0$, and said second fraction $d\beta = m_1$ if $V_q > 0$ and $d\beta = -m_1$ if $V_q < 0$;

in each of a continuous sequence of modulation periods which are small compared with the period of voltage of said AC mains, operating a first pair of said switches for a first fraction, $d\alpha$, of said period, operating a second pair of said switches for a second fraction, $d\beta$, of said period, and operating a set of switches for the remainder of said period;

and further comprising:

50 if $V_d\sqrt{3} < |V_q|$, said first pair of switches include a top switch connected to a third AC main, next advanced in phase from said given one of said AC mains, but if not, then if $V_q > 0$, said first pair of switches include a top switch connected to said given one of said AC mains, but if neither, then said first pair of switches include

- 55 a top switch connected to a second AC main, next delayed in phase from said given one of said AC mains;
- if $V_d\sqrt{3} > |V_q|$, said first pair of switches include a bottom switch connected to said third AC main, but if not, then if $V_q < 0$, said first pair of switches include a bottom switch connected to said
- 60 given one of said AC mains, but if neither, then said first pair of switches include a bottom switch connected to said second AC main;
- if $V_d\sqrt{3} > |V_q|$, said second pair of switches include a top switch connected to said second main, but if not, then if $V_q > 0$, said second pair of switches include a top switch connected to said
- 65 given one of said AC mains, but if neither, then said second pair of switches include a top switch connected to said third AC main; and
- if $V_d\sqrt{3} < |V_q|$, said second pair of switches include a bottom switch connected to said second main, but if not, then if V_q
- 70 < 0 , said second pair of switches include a bottom switch connected to said given one of said AC mains, but if neither, then said second pair of switches include a bottom switch connected to said third AC main.

8. A method according to claim 7 wherein said first fraction of time precedes said second fraction of time within said modulation periods.

9. A method according to claim 7 wherein the remainder of said period follows said first and second fractions of time within said modulation periods.

FIG. 1

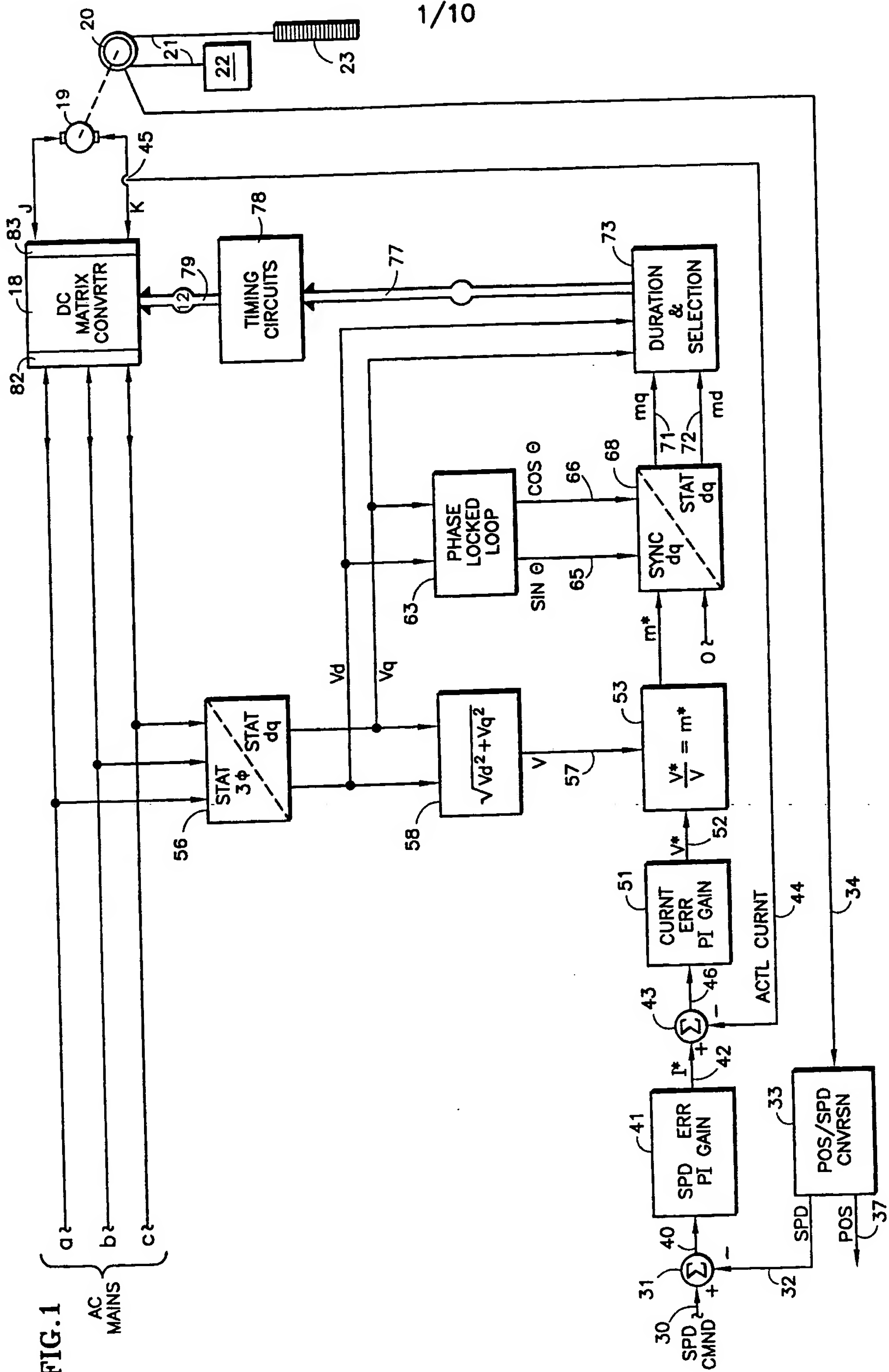


FIG. 2

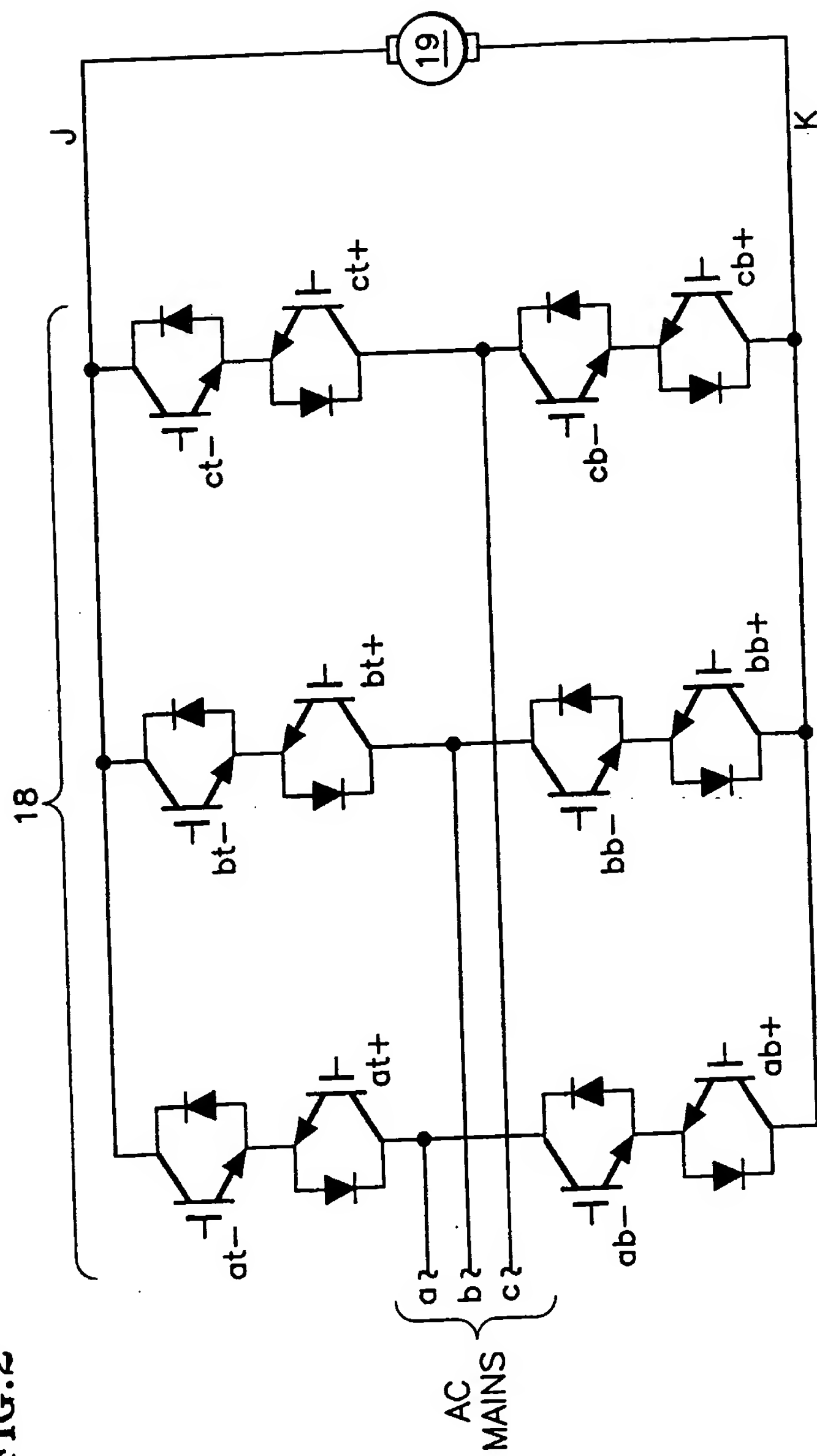
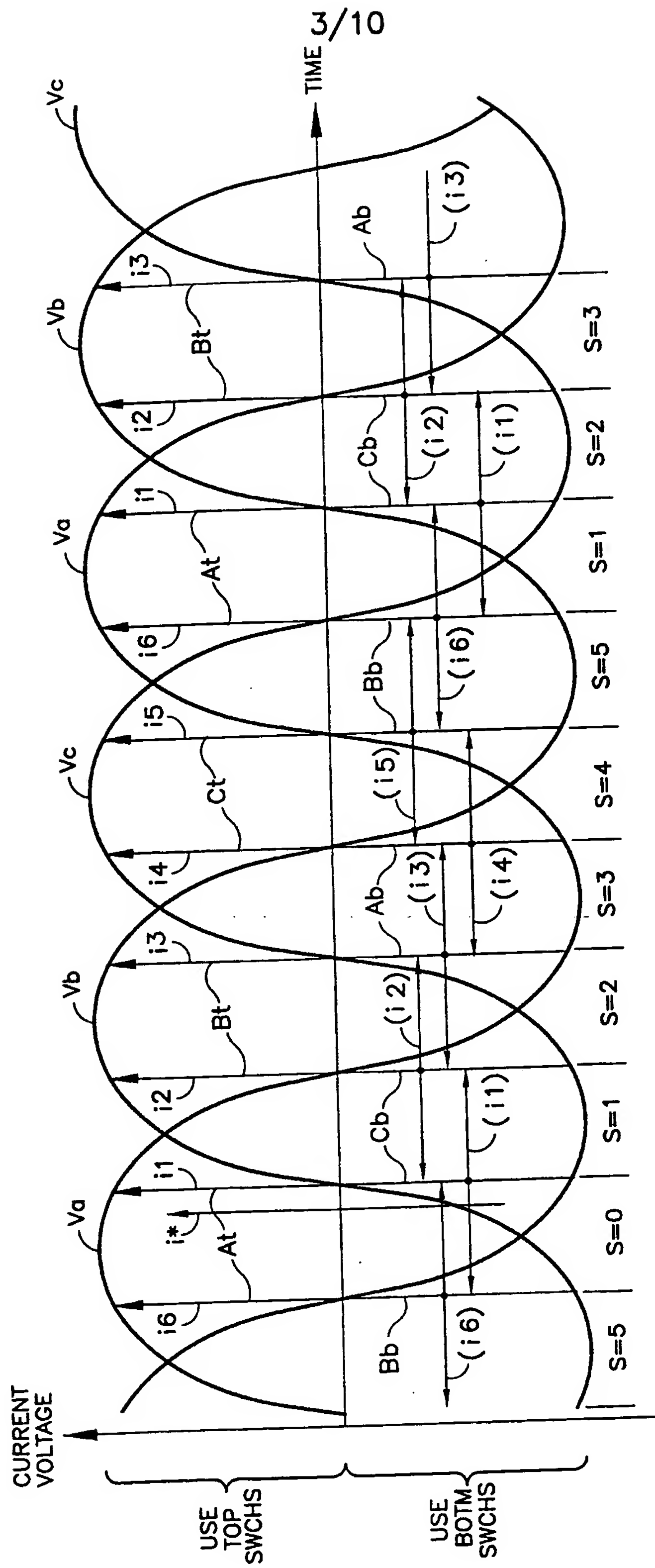


FIG. 3



4/10

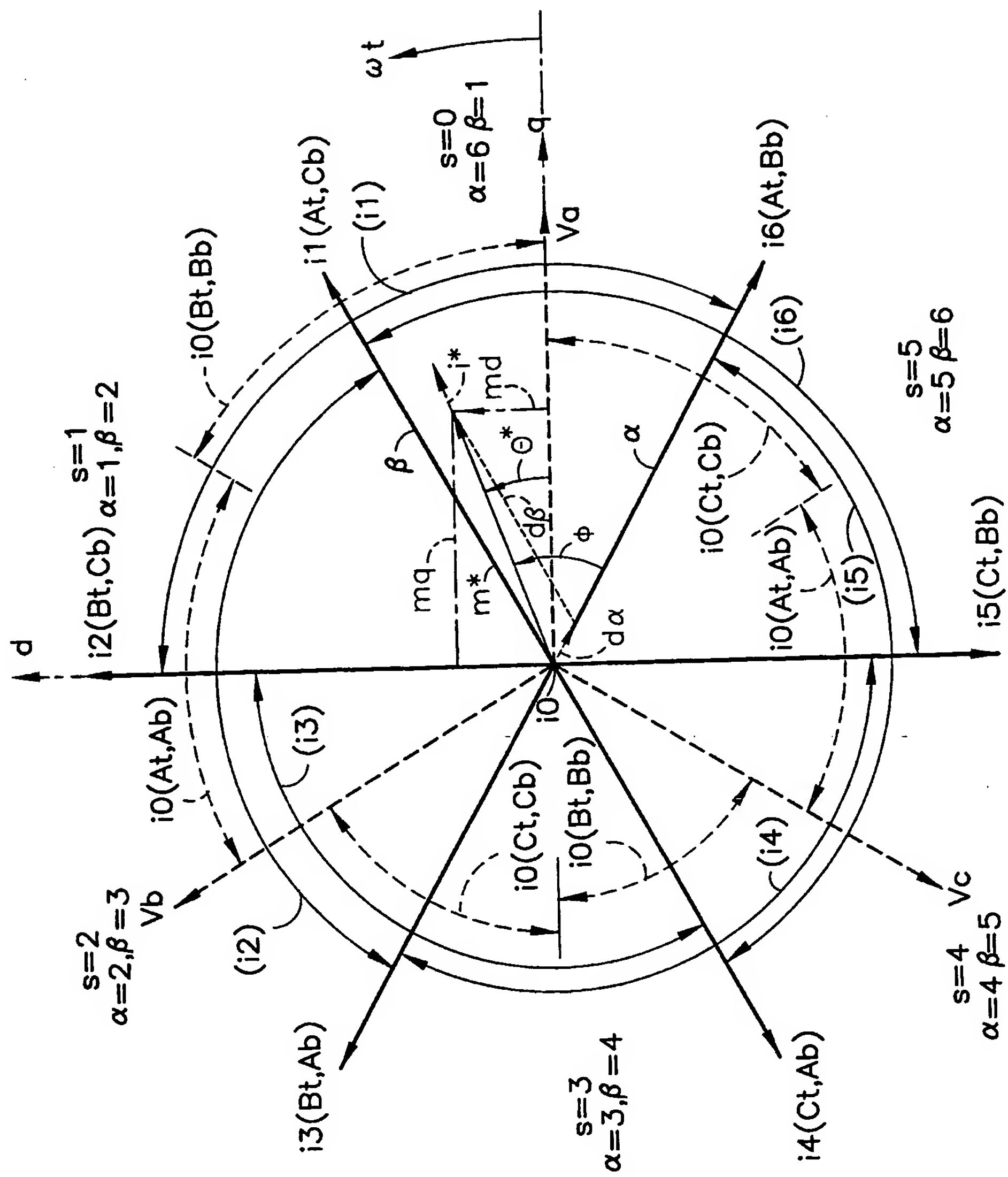


FIG. 4

5/10

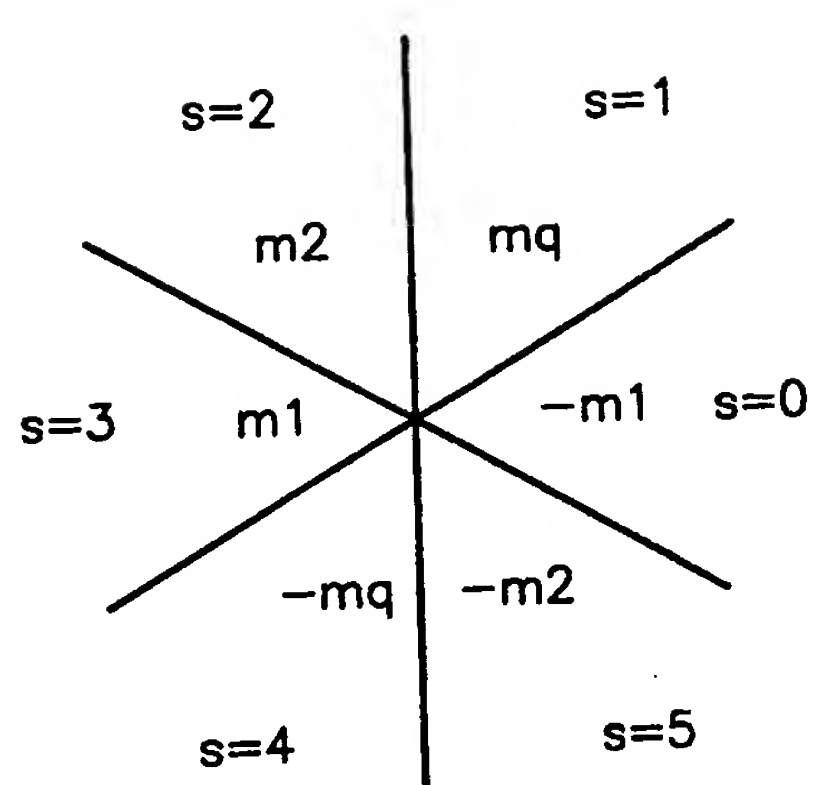
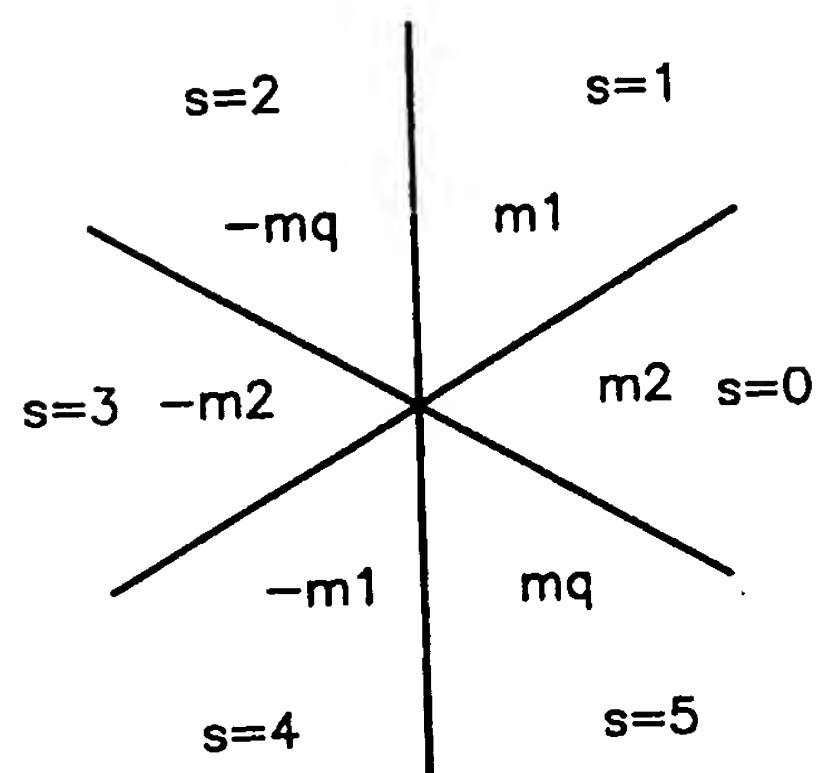
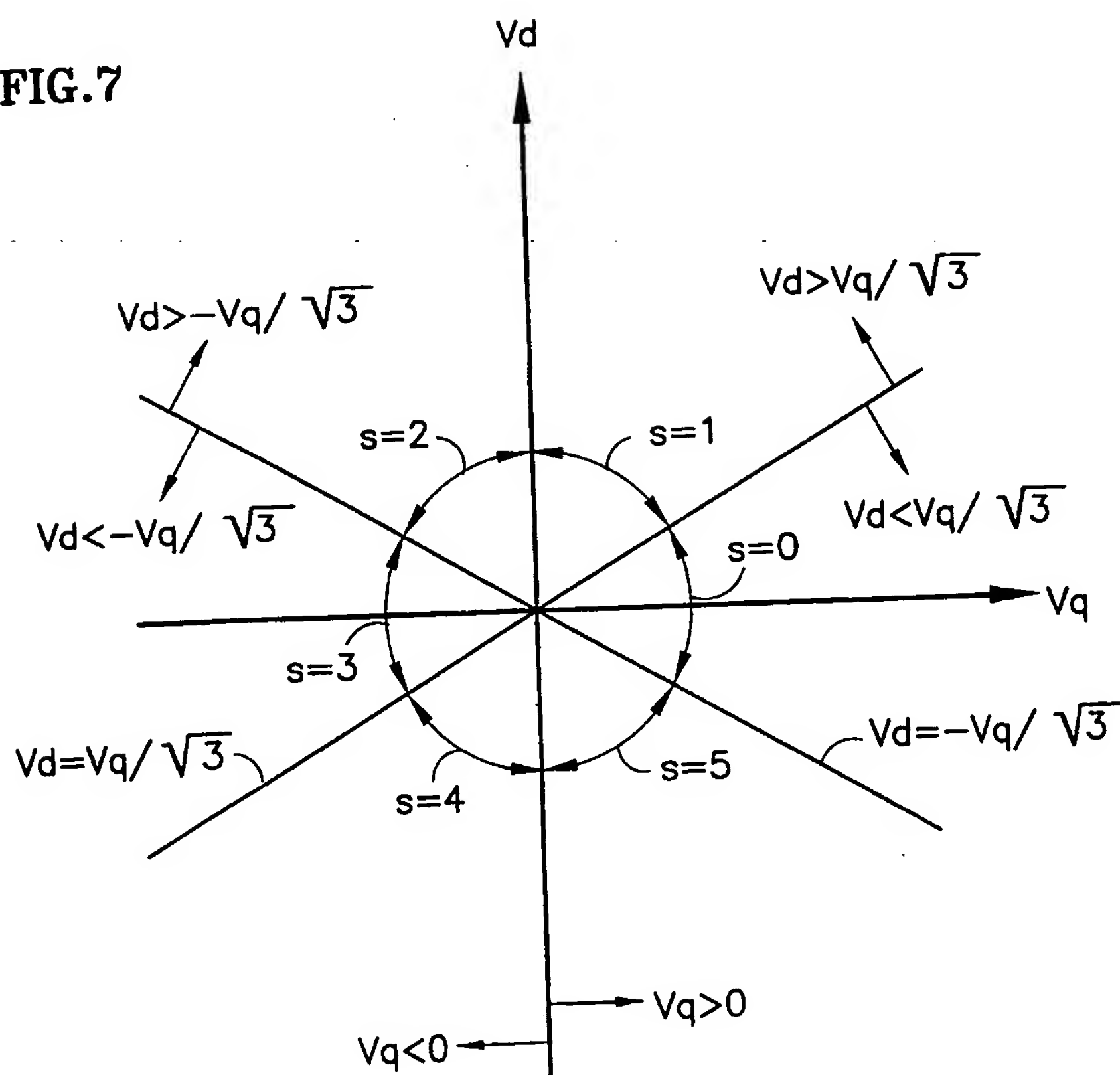
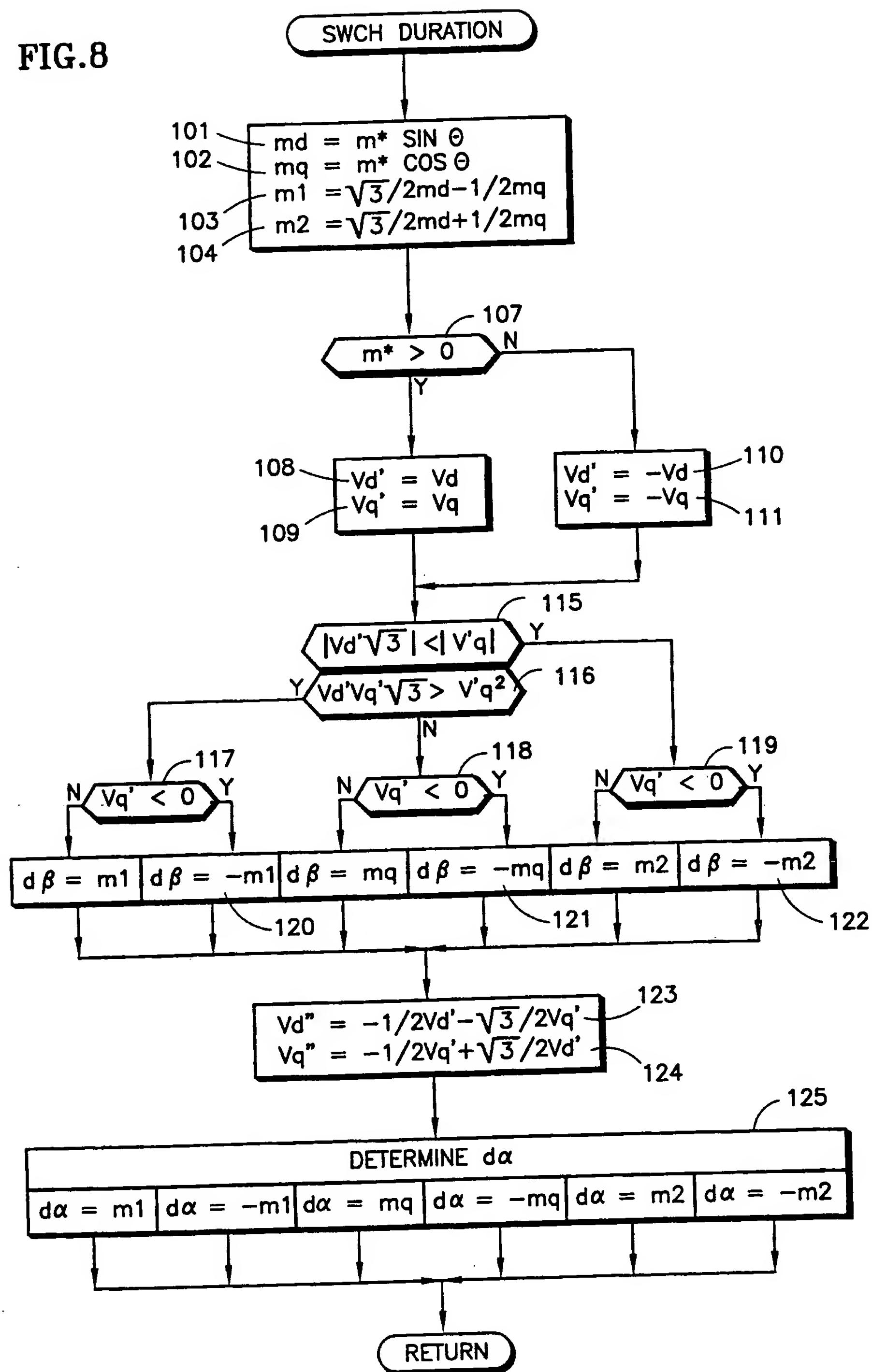
FIG. 5 $d\alpha$ FIG. 6 $d\beta$

FIG. 7



6/10

FIG. 8



7/10

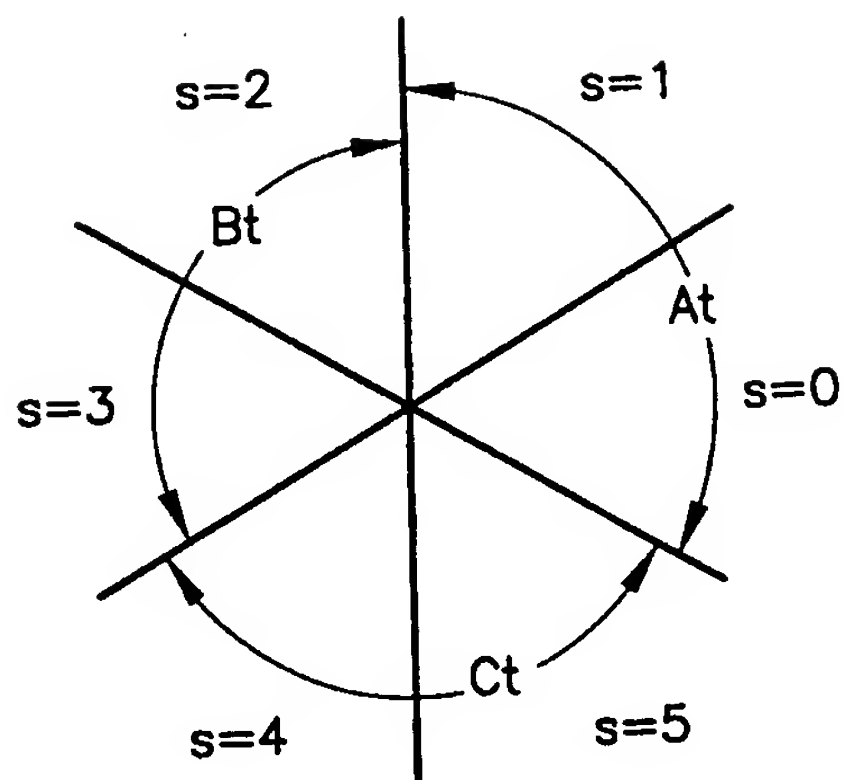


FIG. 9 TOP α SWCH

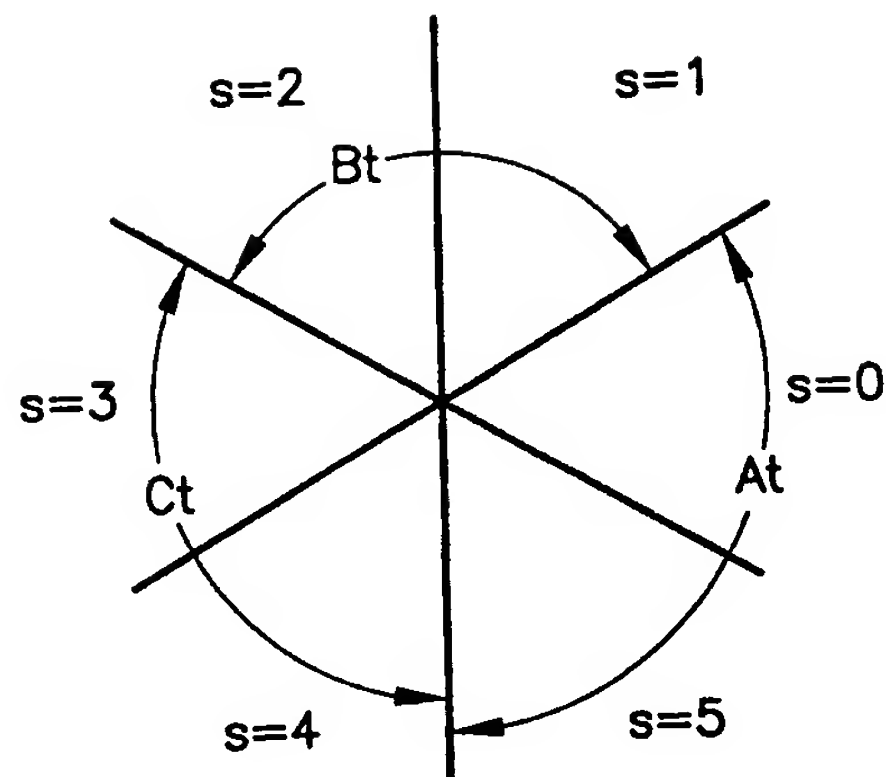


FIG. 10 TOP β SWCH

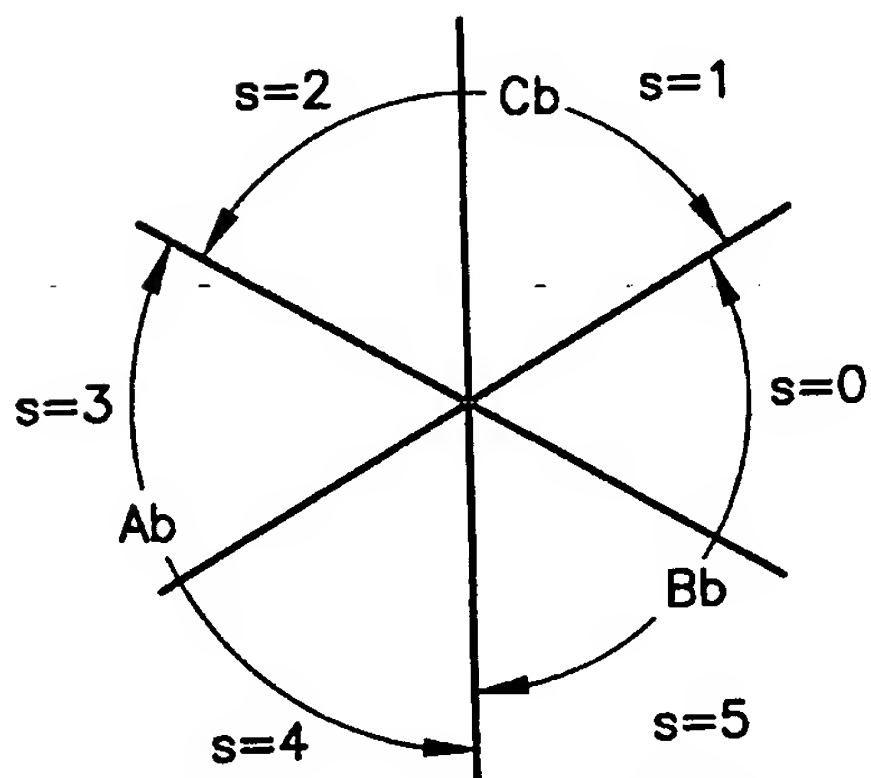


FIG. 11 BOTM α SWCH

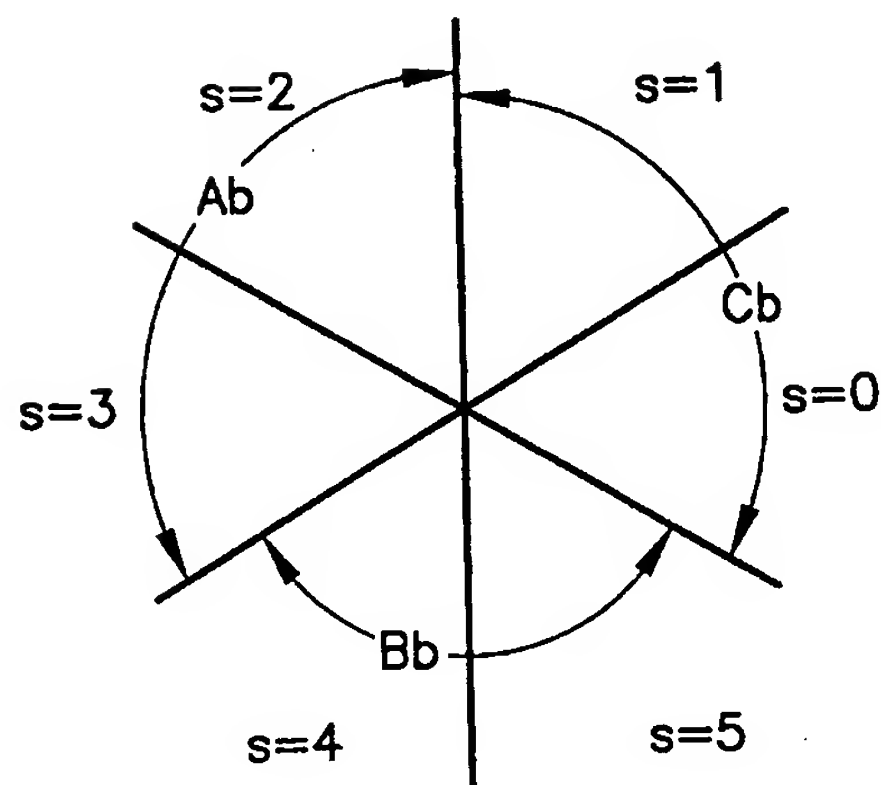
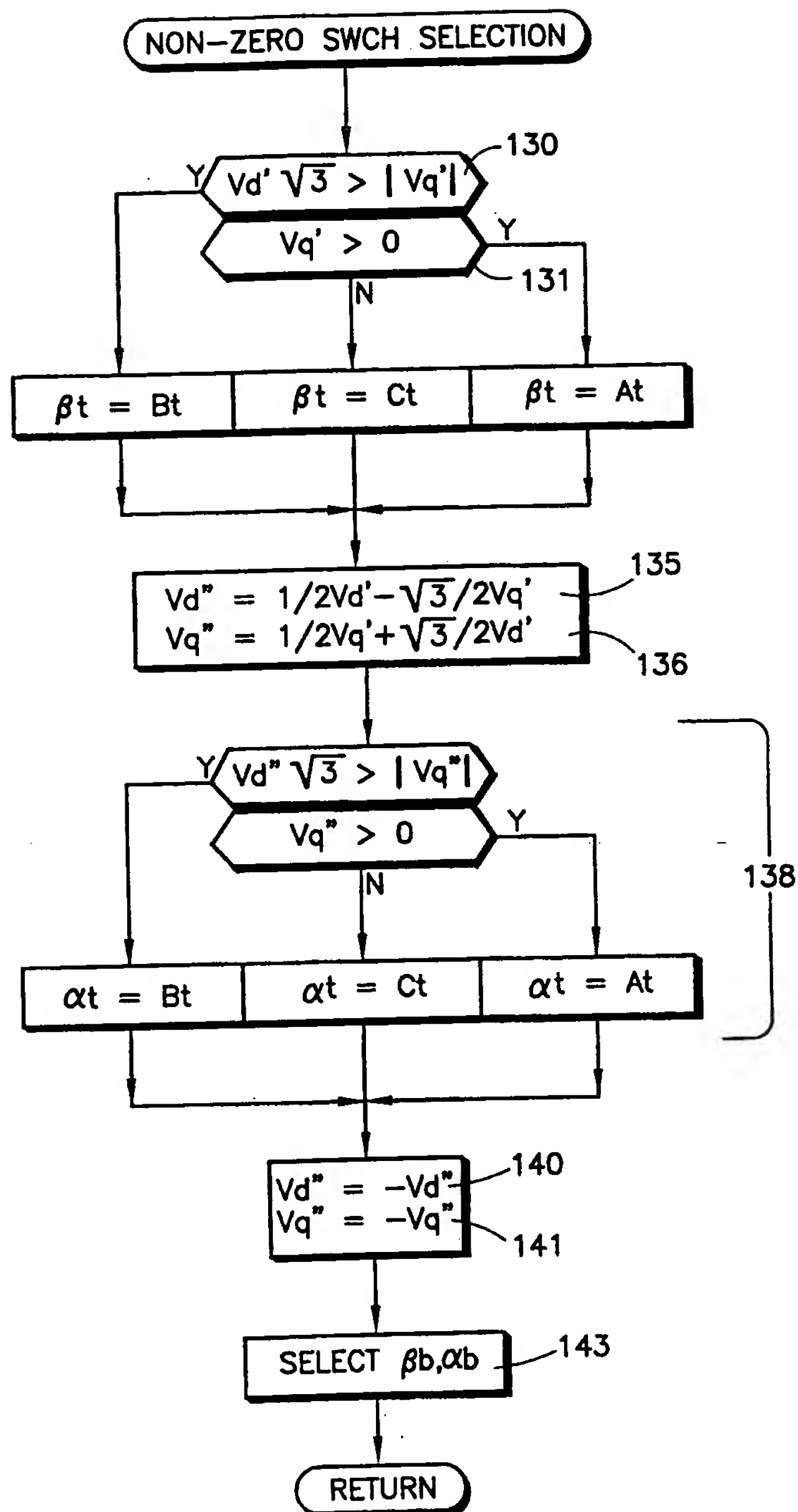


FIG. 12 BOTM β SWCH

8/10

FIG.13



9/10

FIG.14

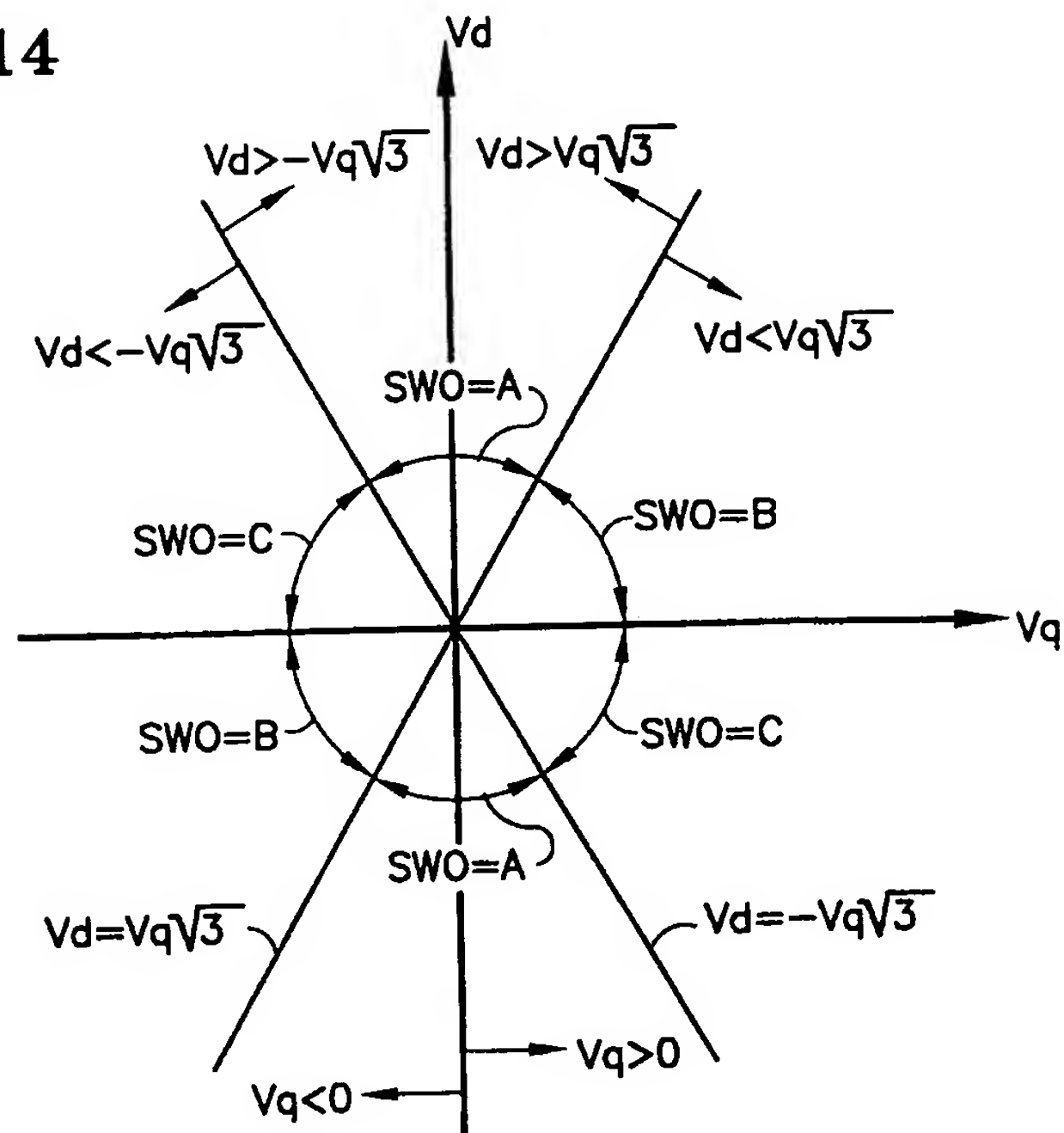
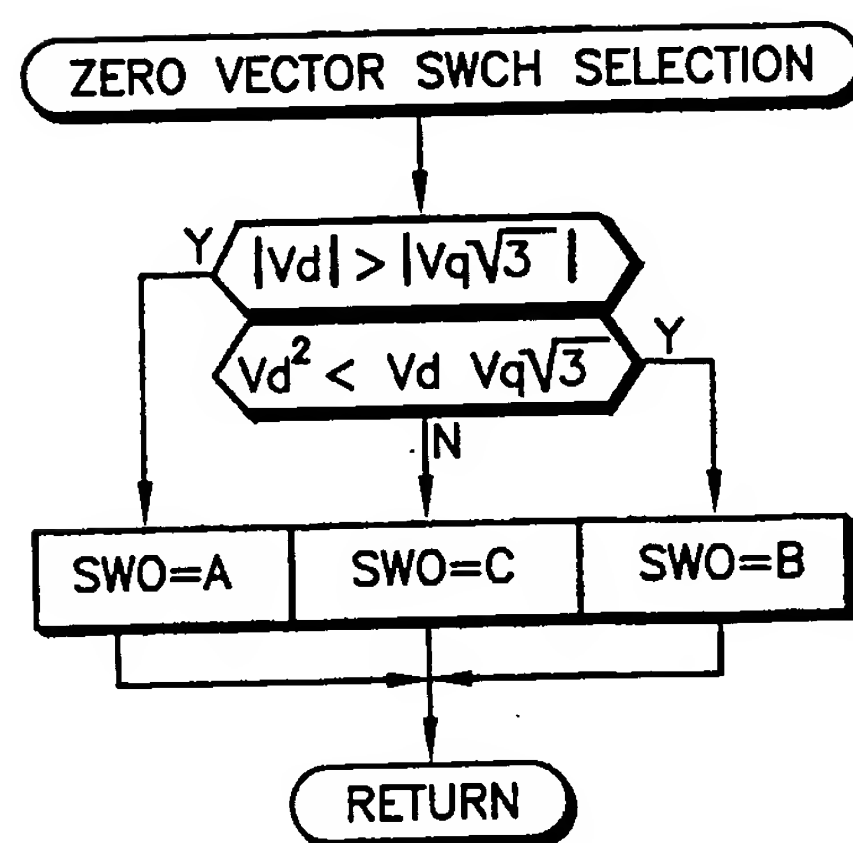


FIG.15



10/10

FIG.16A

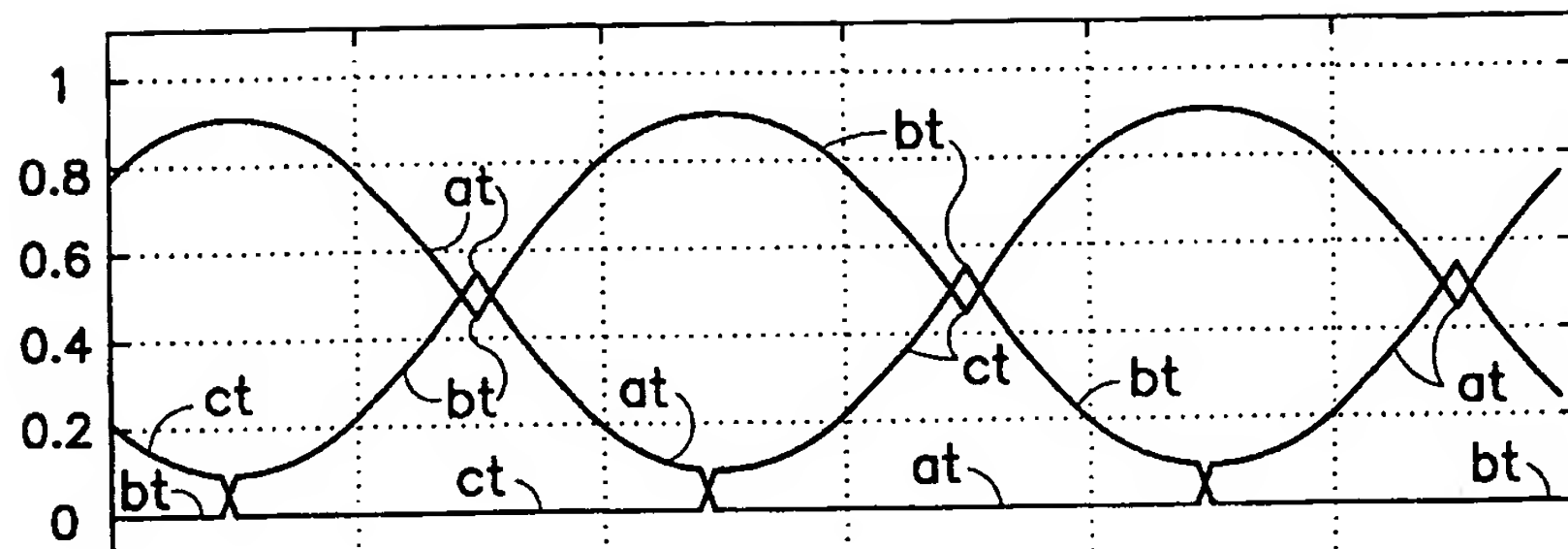


FIG.16B

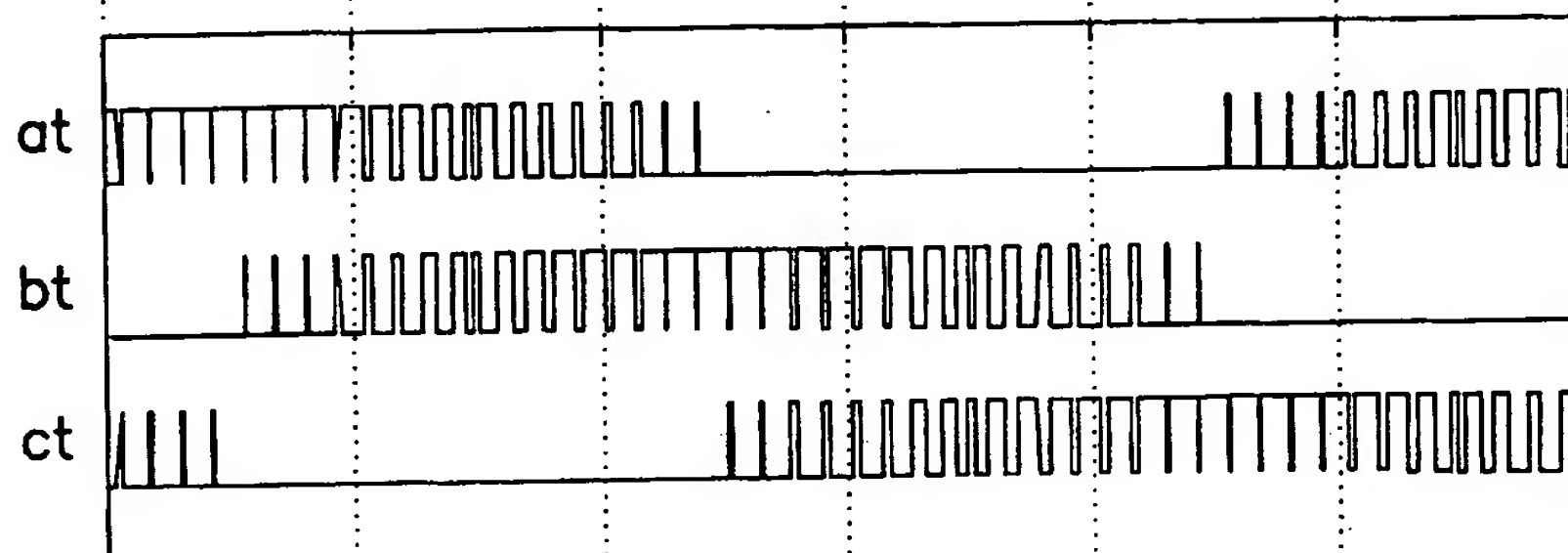
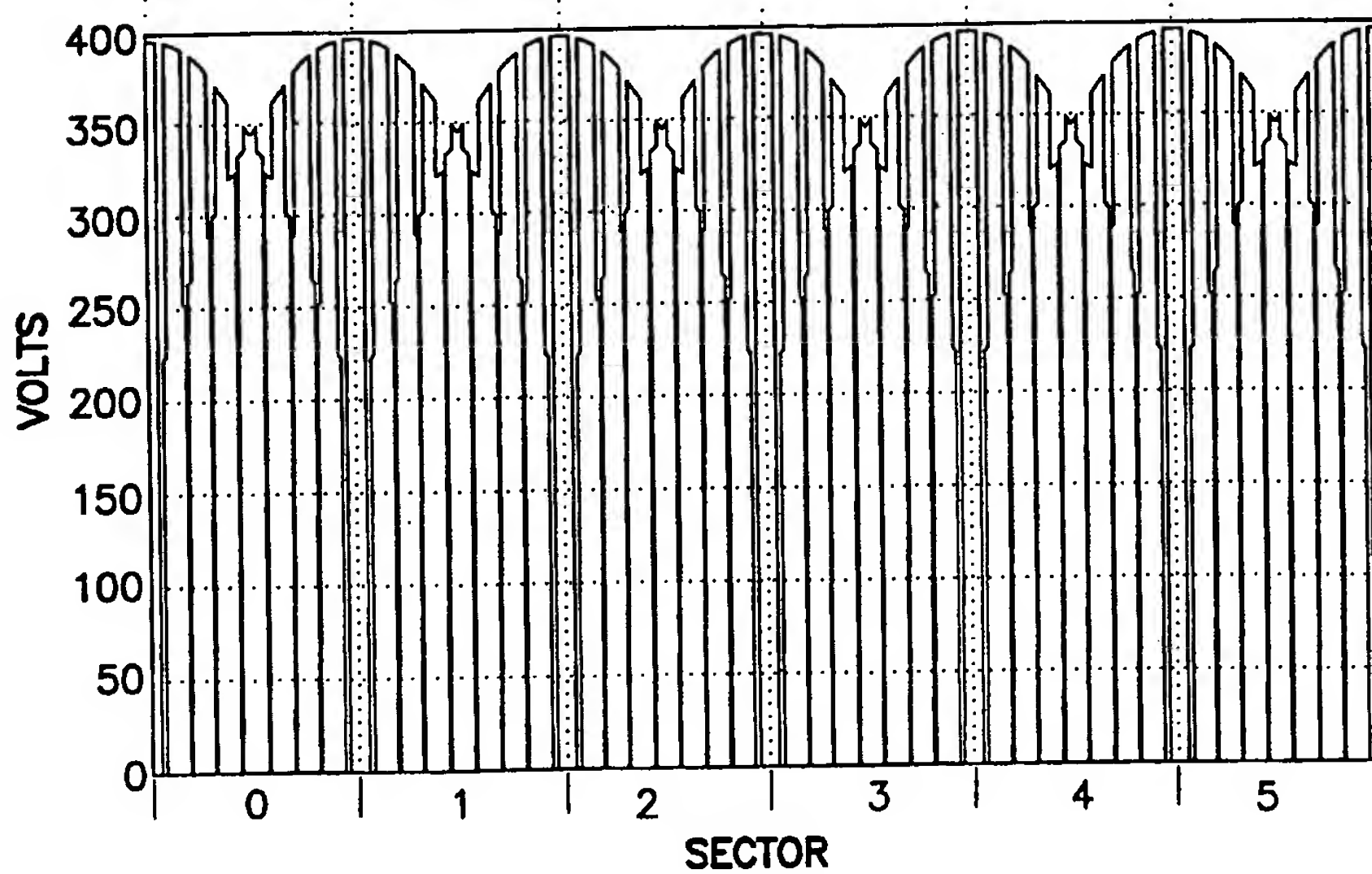


FIG.16C



INTERNATIONAL SEARCH REPORT

Int. Application No

PCT/US 00/12149

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H02M7/162

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4 599 685 A (MITSUYUKI HOMBU ET AL.) 8 July 1986 (1986-07-08) figures 6,10 column 6, line 27 - line 43 column 8, line 10 - line 23 ---	1-9
Y	US 5 706 186 A (A) 6 January 1998 (1998-01-06) figure 11 column 3, line 28 - line 51 ---	1-9
A	US 3 961 154 A (ROLF ERICSON) 1 June 1976 (1976-06-01) figure 8 column 13, line 1 - line 37 ---	1-9
-/--		

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search

5 September 2000

Date of mailing of the international search report

13/09/2000

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International Application No

PCT/US 00/12149

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